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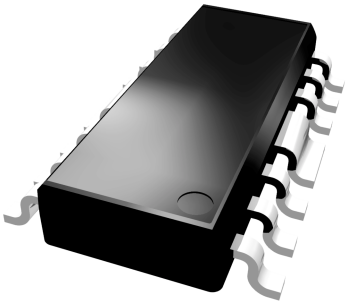
ADA10001

Linear Amplifier MMIC

Data Sheet - Rev 2.2

FEATURES

- High Linearity : +18 dBm IIP3
- Low Noise Figure: 2.0 dB
- Single Supply: +8 VDC
- Wide Bandwidth: 50 MHz to 1 GHz



S3 Package
Modified 16 Pin SOIC

APPLICATIONS

- Driver Amplifier
- CATV - Distribution / Drop Amplifiers

PRODUCT DESCRIPTION

The ADA10001 is a monolithic IC intended for use in applications requiring high linearity, such as Cellular Telephone Base Station Driver Amplifiers, CATV Fiber Receiver and Distribution Amplifiers and CATV Drop Amplifiers. Offered in a modified 16 lead surface mount SOIC package, it is well suited for use in amplifiers where small size, reduced component count, and high reliability are important.

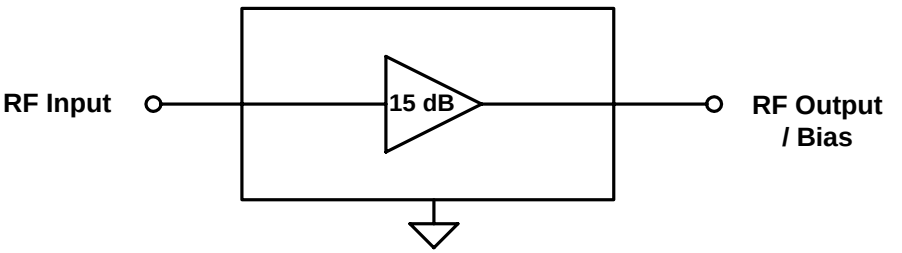


Figure 1: Block Diagram

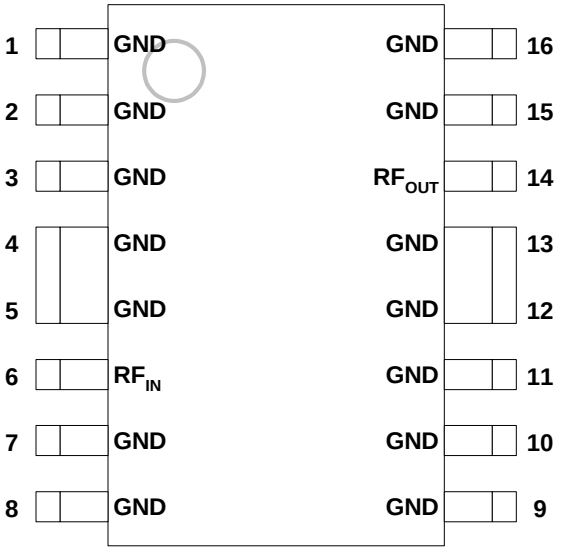


Figure 2: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	GND	Ground	9	GND	Ground
2	GND	Ground	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	GND	Ground
5	GND	Ground	13	GND	Ground
6	RF_{IN}	RF Input	14	RF_{OUT}	RF Output / Supply
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	GND	Ground

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Maximum and Minimum Ratings

PARAMETER	MIN	MAX	UNIT
Supply (pin 14)	0	+12	VDC
RF Power at Input (pin 6)	-	+10	dBm
Storage Temperature	-65	+150	°C
Soldering Temperature	-	260	°C
Soldering Time	-	5	sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Note:

1. Pin 6 should be AC-coupled. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
RF Input / Output Frequency	50	-	1000	MHz
Supply Voltage: V_{DD} (pin 14)	+4	+8	+9	VDC
Case Temperature	-40	-	+85 (1)	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Note:

(1) Median time to failure will degrade above this temperature.

Table 4: Electrical Specifications
(T_A = +25 °C, V_{DD} = + 8 VDC, Test System = 75Ω)

PARAMETER	MIN	TYP	MAX	UNIT
CSO (1)	60	-	-	dBc
CTB (1)	65	-	-	dBc
Gain	14	15	-	dB
Noise Figure	-	2.0	3.5	dB
2nd Order Input Intercept Point (IIP2) (2)	+35	+38	-	dBm
3rd Order Input Intercept Point (IIP3) (2)	+15	+18	-	dBm
Thermal Resistance	-	-	35	°C/W
Current Consumption (3)	50	-	150	mA

Notes:
(1) 160 channels, +23 dBmV per channel (measured at output), 6 MHz channel spacing
(2) Two tones, -10 dBm per tone at input
(3) The device can be operated at V_{DD} = +6 VDC for lower power dissipation. Refer to the figures on page 5 for performance variation with supply voltage.

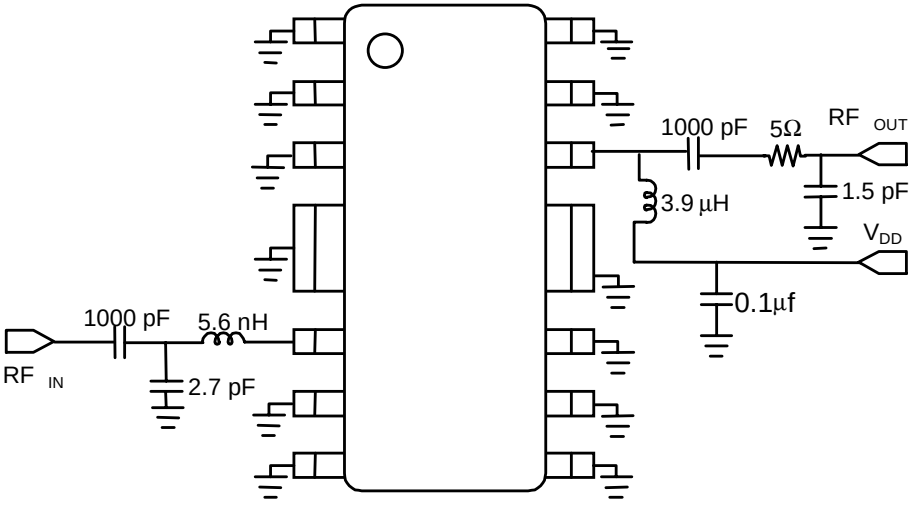


Figure 3: Test Circuit

PERFORMANCE DATA

Figure 4: Gain Noise Figure vs. Frequency

T_A = 25 °C, V_{DD} = +8V

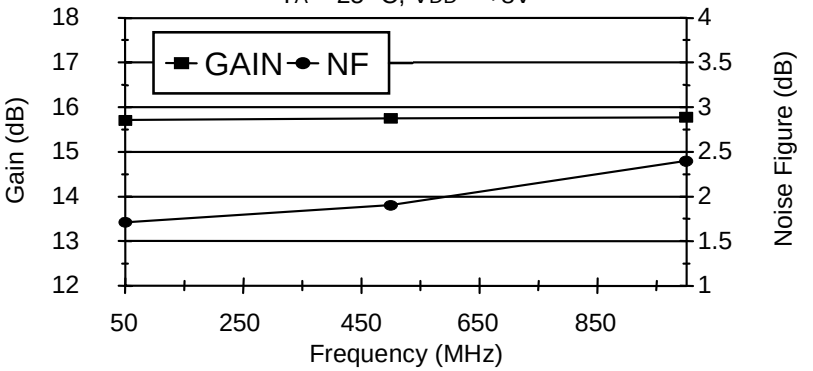


Figure 5: Gain and Noise Figure vs. V_{DD}

T_A = 25 °C, RF = 500 MHz

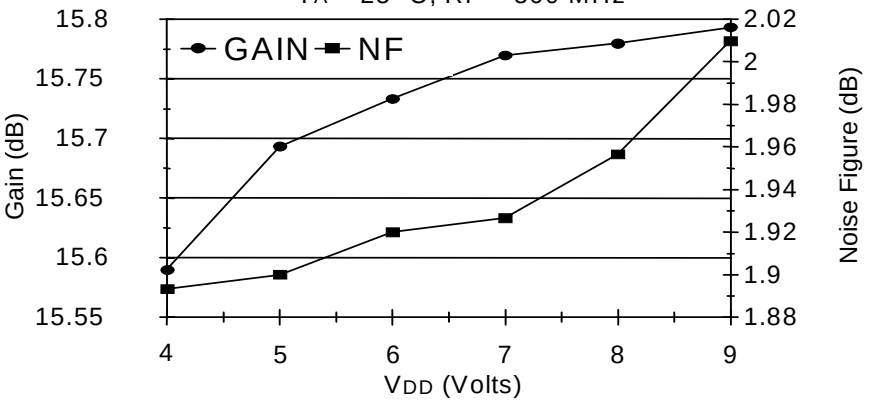
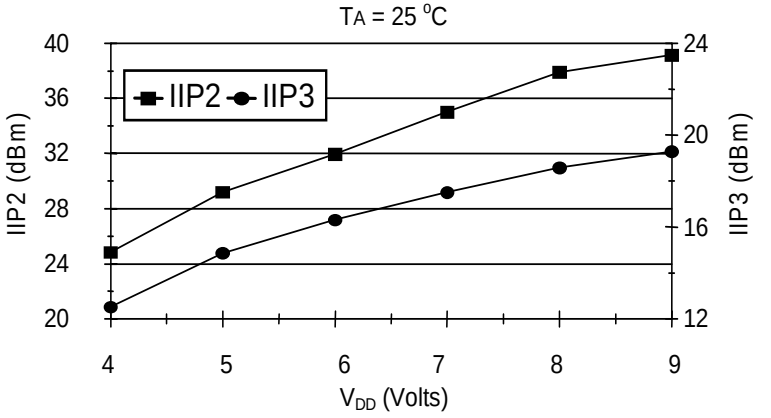


Figure 6: IIP2, IIP3 vs. V_{DD}

T_A = 25 °C



Notes:

1. *IIP2 measured at 986.5 MHz; Input = two tones at 55.25 MHz and 931.25 MHz at -10 dBm.*
2. *IIP3 measured with two tones at the input: 986.5 MHz and 992.5 MHz at -10 dBm.*

Figure 7: Output Power vs. Input Power

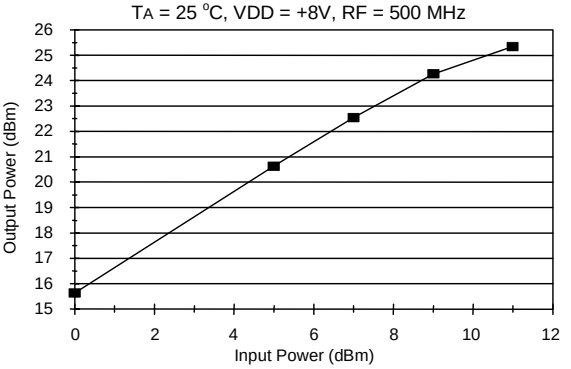
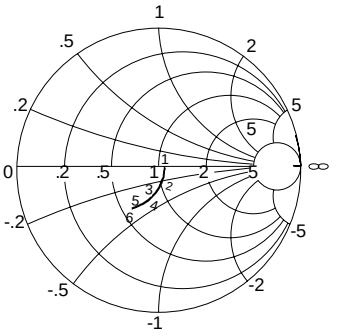


Figure 8: Input Impedance

START: 0.050 GHz
STOP: 1.00 GHz



1: 0.050 GHz
79.76 Ω
- 4.79 jΩ

2: 0.20 GHz
77.88 Ω
- 13.21 jΩ

3: 0.40 GHz
70.02 Ω
- 21.83 jΩ

4: 0.6 GHz
59.63 Ω
- 26.56 jΩ

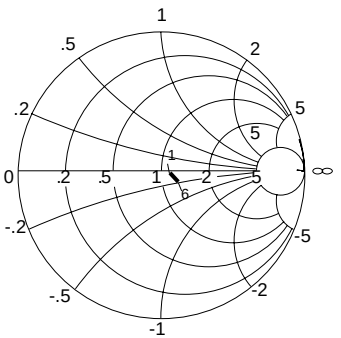
5 : 0.8 GHz
49.91 Ω
- 26.56 jΩ

6: 1.0 GHz
41.77 Ω
- 25.15 jΩ

Measured in 75 Ω System

Figure 9: Output Impedance

START: 0.050 GHz
STOP: 1.00 GHz



1: 0.050 GHz
83.9 Ω
- 8.1 jΩ

2: 0.20 GHz
84.17 Ω
- 1.19 jΩ

3: 0.40 GHz
85.38 Ω
- 2.27 jΩ

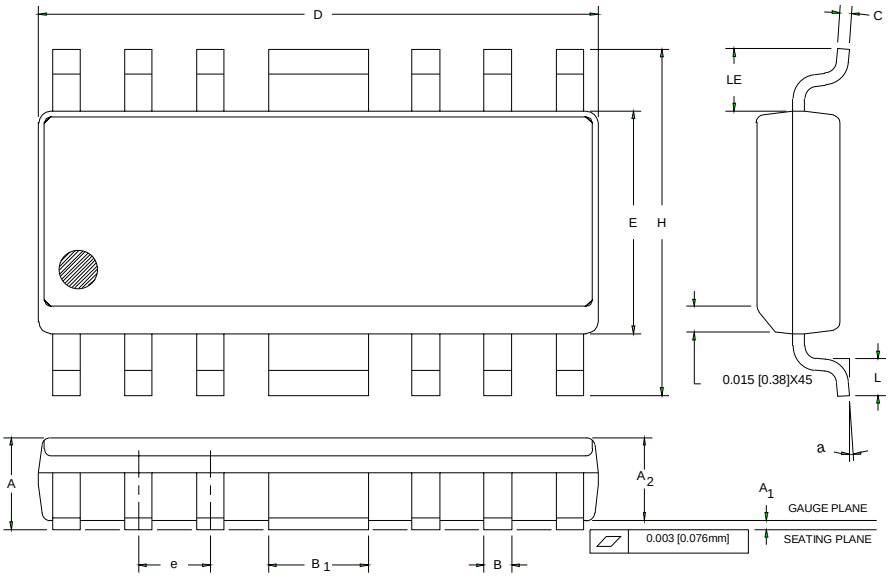
4: 0.6 GHz
87.64 Ω
- 3.82 jΩ

5 : 0.8 GHz
90.20 Ω
- 6.60 jΩ

6: 1.0 GHz
93.57 Ω
- 11.76 jΩ

Measured in 75 Ω System

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A_1	0.004	0.010	0.10	0.25	
A_2	0.055	0.065	1.40	1.65	
B	0.013	0.020	0.33	0.50	
B_1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050 BSC		1.27 BSC		
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	——	0.76	——	
a	0	8	0	8	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.

Figure 10: S3 Package Outline - Modified 16 Pin SOIC

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ADA10001S3CTR	-40 °C to +85 °C	Modified 16 Pin SOIC	3,500 piece Tape and Reel
ADA10001S3C	-40 °C to +85 °C	Modified 16 Pin SOIC	Plastic tubes (50 pieces per tube)